WHAT IS CLAIMED IS:

1. A memory device, comprising:

a plurality of fins formed adjacent to one another, at least one of the fins being doped with a first type of impurities and at least one other one of the fins being doped with a second type of impurities;

a source region formed at one end of each of the fins;

a drain region formed at an opposite end of each of the fins;

a gate formed over two of the plurality of fins;

a wordline formed over each of the plurality of fins; and

a bitline contact formed adjacent at least one of the plurality of fins.

2. The memory device of claim 1, wherein a width of each of the fins ranges from about 50 Å to about 500 Å.

3. The memory device of claim 1, wherein a height of each of the fins ranges from about 50 Å to about 500 Å.

4. The memory device of claim 1, wherein the plurality of fins includes four fins.

5. The memory device of claim 1, wherein a first pair of the plurality of fins is doped with a first type of impurities and the second pair of the plurality of fins is doped with a second type of impurities.

6. The memory device of claim 1, wherein the first type of impurities includes n-type

impurities and the second type of impurities includes p-type impurities.

7. A method of doping fins of a semiconductor device that includes a substrate, the method comprising:

forming a plurality of fin structures on the substrate, each of the fin structures including a cap formed on a fin;

performing a first tilt angle implant process to dope a first pair of the plurality of fin structures with n-type impurities; and

performing a second tilt angle implant process to dope a second pair of the plurality of fin structures with p-type impurities.

8. The method of claim 7, wherein a width of each of the fin structures ranges from about 50 Å to about 500 Å.

9. The method of claim 7, wherein a first distance between a first fin structure of the plurality of fin structures and a second fin structure of the plurality of fin structures ranges from about 100 Å to about 1000 Å and a second distance between the second fin structure and a third fin structure of the plurality of fin structures ranges from about 200 Å to about 2000 Å.

10. The method of claim 7, wherein a height of each of the fins ranges from about 50 Å to about 500 Å.

11. The method of claim 7, wherein the first tilt angle implant process is performed at an angle ranging from about 40 degrees to about 50 degrees.

12. The method of claim 7, wherein the second tilt angle implant process is performed at an angle ranging from about 40 degrees to about 50 degrees.

13. The method of claim 7, further comprising:

performing a third tilt angle implant process to further dope the first pair of the plurality of fin structures with n-type impurities; and

performing a fourth tilt angle implant process to further dope the second pair of the plurality of fin structures with p-type impurities.

14. The method of claim 13, wherein the third tilt angle implant process is performed at an angle ranging from about 40 degrees to about 50 degrees.

15. The method of claim 13, wherein the fourth tilt angle implant process is performed at an angle ranging from about 40 degrees to about 50 degrees.

16. The method of claim 13, further comprising:

forming hardened resists on non-shadowed side surfaces of the first and second pairs of the plurality of fin structures prior to performing the third and fourth tilt angle implant processes.

17. A method for forming a memory device, comprising:

forming a plurality of fins adjacent to one another, at least one of the fins being doped with a first type of impurities and at least one other one of the fins being doped with a second type of impurities;

forming a source region at one end of each of the fins;

forming a drain region at an opposite end of each of the fins;

forming a gate over two of the plurality of fins;

forming a wordline over each of the plurality of fins; and

forming a bitline contact adjacent at least one of the plurality of fins.

18. The method of claim 17, wherein the memory device comprises a static random access memory (SRAM).

19. The method of claim 17, wherein the plurality of fins are formed in pairs.

20. The method of claim 19, wherein fins of each pair of the pairs are formed a distance of approximately 100 Å apart.